

Interfacing the HCTL-1100 to the 8051



Application Brief M-015

HCTL-1100/8051

Interfaces

This application brief offers two different approaches to interfacing the HCTL-1100 to the 8051 microcontroller family. The first approach uses the 8051's address/data/control bus to communicate with the HCTL-1100 and the second approach uses the 8051's I/O ports to communicate with the HCTL-1100.

The choice of which interface is most appropriate for your application should be based on whether or not your current design is utilizing the 8051's bus structure. If your 8051 design is utilizing the bus, it makes sense to use the HCTL-1100 bus interface circuit. This approach requires only two additional TTL chips. If your 8051 design is completely I/O based with no external memory, it makes sense to use the I/O port interface. The I/O interface requires no additional glue logic.

The I/O routines are slightly more complicated for the I/O interface than for the bus interface. These routines can

be seen in the software listings provided with this application brief. There is only a marginal performance difference between the two approaches. The execution times for these routines are listed in Table 1.

These execution times do not include stack operations and subroutine overhead.

The HCTL-1100 bus interface circuit is capable of supporting four HCTL-1100s with no additional logic. If an I/O port based design requires more than one HCTL-1100, the interface would require only two additional I/O port lines per chip. These lines would control OE (Output Enable) and CS (Chip Select) for each of the individual HCTL-1100s. If there is an inadequate number of I/O port lines available for this purpose, a separate decoder chip could be used. One such chip is the 74LS138 3-to-8 decoder which is capable of handling four HCTL-1100s.

Table 1. Execution Times

	Read Operation	Write Operation
I/O Port Interface	15 ms at 12 MHz 180 Clock Per.	13 ms at 12 MHz 156 Clock Per.
Bus Interface	12 ms at 12 MHz 144 Clock Per.	6 ms at 12 MHz 72 Clock Per.

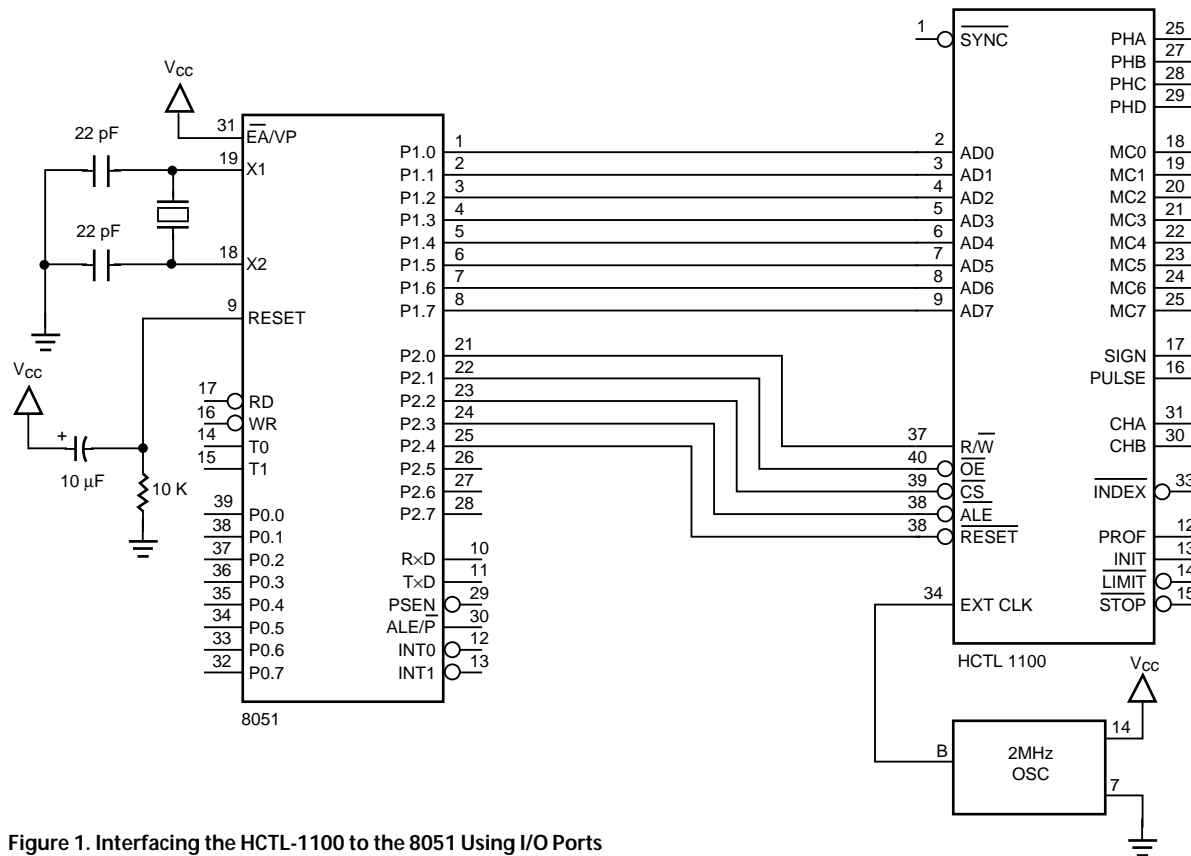


Figure 1. Interfacing the HCTL-1100 to the 8051 Using I/O Ports

```

;*****
;HCTL-1100 READ/WRITE ROUTINES
;THIS SOFTWARE IS USED IN CONJUNCTION WITH THE HCTL-1100/8051 I/O
;PORT INTERFACE
;*****

;*****
;SUBROUTINE RD1100
;READS HCTL REG POINTED TO BY B AND RETURNS REG VALUE IN ACC
;*****
RD1100:  SETB    P2.0        ; SET R/W LINE TO READ

        MOV     P1,B        ; LATCH ADDRESS
        CLR    P2.3        ; PULSE ALE
        SETB   P2.3
        MOV    P1,#0FFH

        CLR    P2.2        ; PULSE CS
        SETB   P2.2
        NOP                    ; DELAY 4µS
        NOP                    ; ALLOW ENOUGH TIME FOR 1MHz
        NOP                    ; HCTL-1100 OR FASTER

        CLR    P2.1        ; SET OE=0
        MOV    A,P0        ; GET DATA FROM 1100
        SETB   P2.1        ; SET OE=1

        RET

```

(Continues)

```

;*****
;SUBROUTINE WR1100
;LOADS HCTL-1100 REGISTER POINTED TO BY B WITH VALUE IN ACC
;*****

```

```

WR1100:  MOV    P1,B      ; LATCH ADDR
         CLR    P2.3    ; PULSE ALE
         SETB   P2.3
         MOV    P1,#0FFH

         CLR    P2.0    ; SET R/W LINE TO WRITE
         MOV    P1,A    ; SEND DATA
         CLR    P2.2    ; PULSE CS
         SETB   P2.2
         SETB   P2.0    ; RETURN R/W TO READ MODE
         MOV    P1,#0FFH

         RET

```

```

;*****
;SUBROUTINE RS1100
;THIS SUBROUTINE RESETS THE HCTL-1100 WITH A 5µS PULSE. THIS IS
;ENOUGH TIME TO RESET A 1MHz HCTL-1100 OR FASTER.
;*****

```

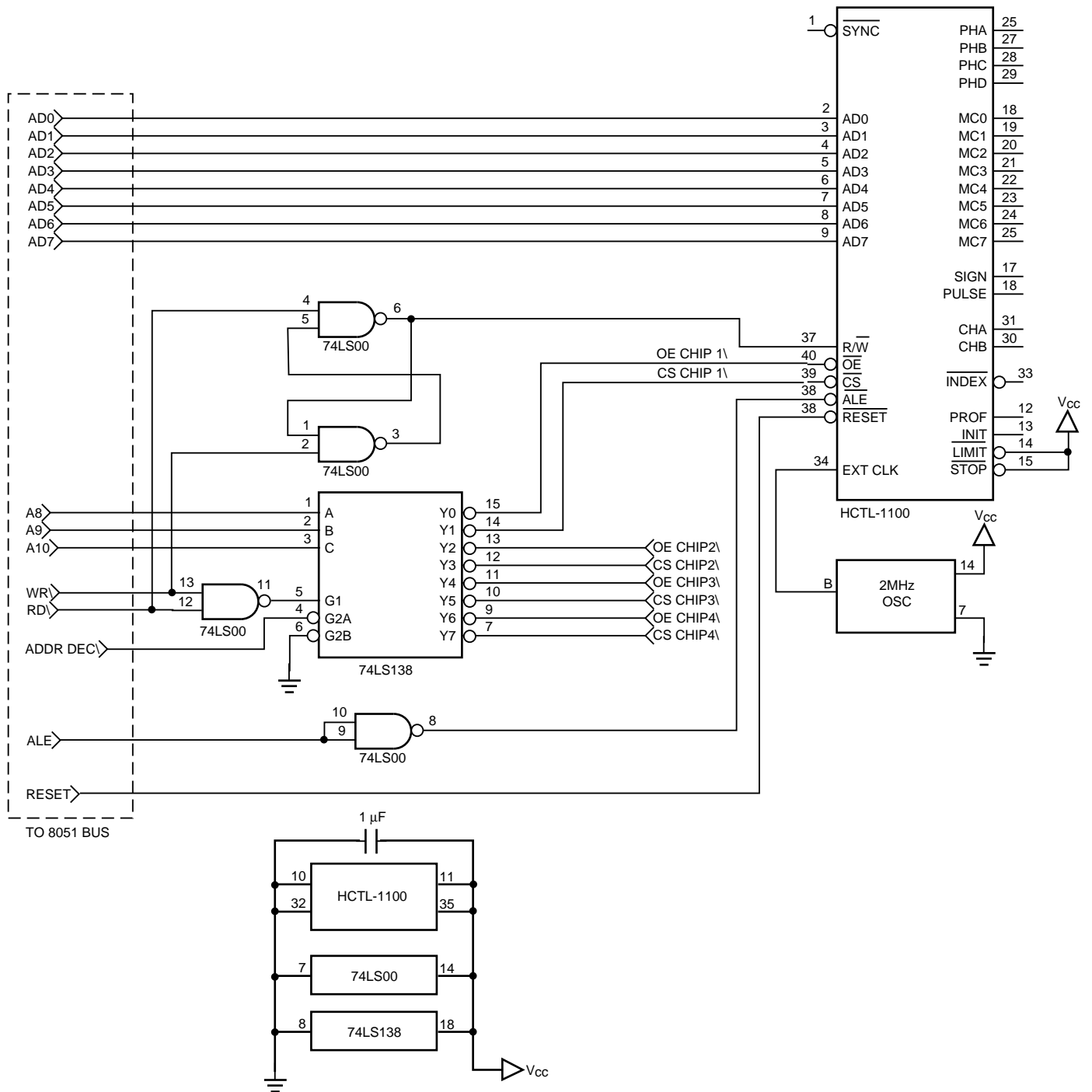
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RS1100:  ORL    P2,#0FH   ; SET R/W TO READ, OE=1, CS=1, AE=1
         MOV    P0,#0FFH ; SET P1=HIGH

         CLR    P2.4    ; SET RESET LOW
         NOP    ; PULSE FOR 5µS
         NOP    ; CAN REMOVE 2 NOP'S FOR 2MHz HCTL-1100
         NOP
         NOP
         SETB   P2.4    ; BRING RESET LINE HIGH

         RET

```



\ DENOTES AN ACTIVE LOW SIGNAL

Figure 2. Interfacing the HCTL-1100 to the 8051 Using the Address/Data Bus.

```

;*****
;HCTL-1100 READ/WRITE ROUTINES
;THIS SOFTWARE IS USED IN CONJUNCTION WITH THE HCTL-1100
;BUS INTERFACE
;*****

```

```

; HCTL-1100 ADDRESS
OE1100 EQU 060H ; BASE ADDRESS = 6000H
CS1100 EQU 061H ; BASE ADDRESS = 6100H

```

```

;*****
;SUBROUTINE RD1100
;READS HCTL REG POINTED TO BY B AND RETURNS REG VALUE IN ACC
;*****

```

```

RD1100:  PUSH   DPL           ; SAVE DATA POINTER
         PUSH   DPH

         MOV    DPH,#CS1100 ; POINT TO BASE CS ADDRESS
         MOV    DPL,B       ; LOAD REG ADDRESS IN
                               ; LOWER 8 BITS OF DATA POINTER
         MOVX   A,@DPTR     ; LATCH HCTL-1100 REG ADDRESS

         NOP                    ; ALLOW ENOUGH TIME FOR 1MHz CLK
         NOP                    ; (NOT REQUIRED FOR 2MHz HCTL-1100 CLK)
         MOV    DPH,#OE1100 ; POINT TO BASE OE ADDRESS
         MOVX   A,@DPTR     ; READ BYTE FROM HCTL-1100

         POP    DPH         ; RESTORE DATA POINTER
         POP    DPL
         RET

```

```

;*****
;SUBROUTINE WR1100
;LOADS HCTL-1100 REGISTER POINTED TO BY B WITH VALUE IN ACC
;*****

```

```

WR1100:  PUSH   DPL           ; SAVE DATA POINTER
         PUSH   DPH

         MOV    DPTR,#CS1100 ; POINT TO BASE CS ADDRESS
         MOV    DPL,B       ; LOAD REG ADDRESS IN
                               ; LOWER 8 BITS OF DATA POINTER
         MOVX   @DPTR,A     ; WRITE BYTE TO HCTL-1100

         POP    DPH         ; RESTORE DATA POINTER
         POP    DPL
         RET

```

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